



NANOPHOTO Final meeting

Work Package 4 *Prototyping and characterization*





Outline

- Work package overview
- P-type and intrinsic layer characterisation
- PIN Solar cell fabrication process
- IV curves
 - Merten collection model
 - Results
- Conclusion





Work Package Overview

Task 4.1

Fabrication of opto-electronic devices and preliminary characterization and testing

Task 4.2

Characterisation of opto-electronic devices

Remark: Focused on development and characterisation of nc-Si thin-film solar cells





PIN-Si thin-film solar cell „Superstrate“ Configuration

Back contact: Ag or Ti

n-type nc-Si 30-60 nm

intrinsic nc-Si 1-4 μm

p-type nc-Si 30-60 nm

ZnO:Al 1 μm

Glass 1 mm





Space Charge Limited Current (SCLC) case of material with deep traps in a band tail

- If there is a density of traps \gg density of free carriers
- Uniformly spatially distributed
- With an energy distribution such as: $g(E) = A * \exp((E_t - E_c)/kT_c)$
with T_c characteristic temperature of the band tail $T_c \geq T_{\text{measurement}}$

→ The excess injected carriers will fill some traps of the band tail

In this case it has been demonstrated that :

→ $I = A * V^\gamma$ with $\gamma = 1 + T_c/T$

$\gamma \geq 2$ function of the temperature

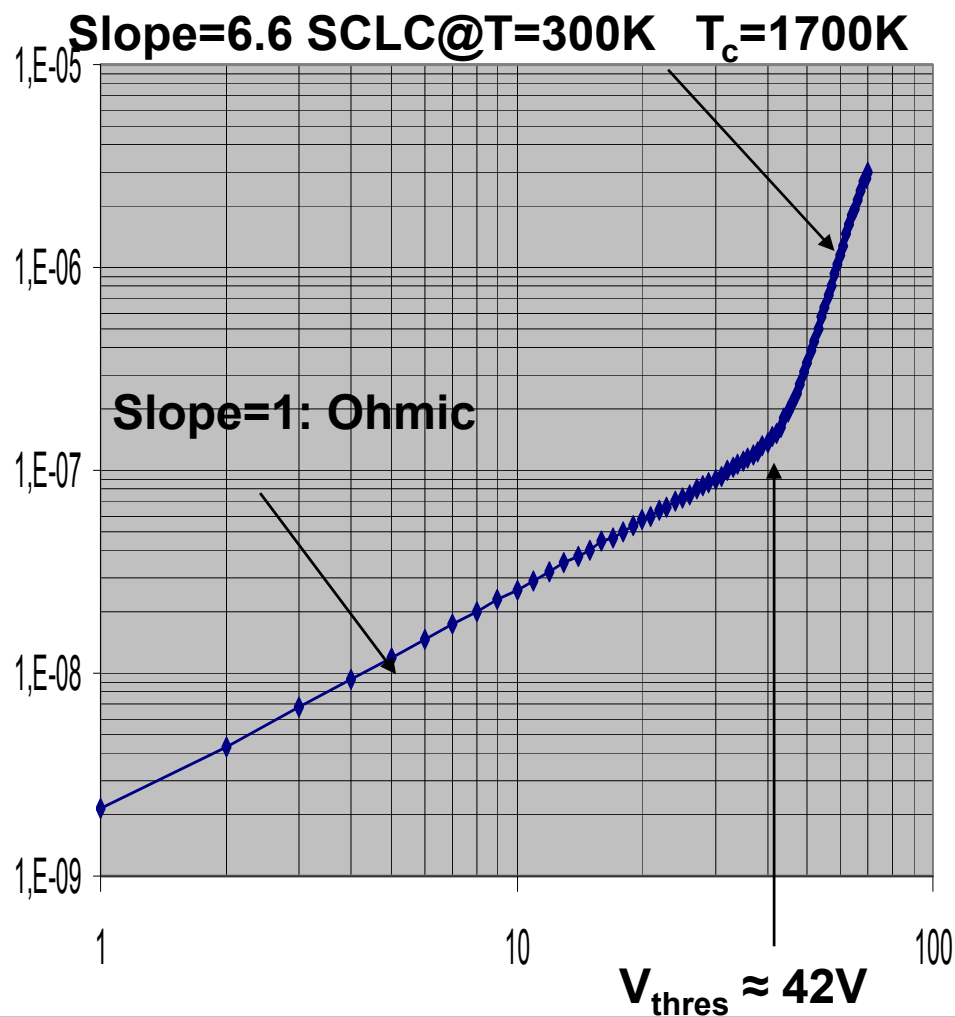
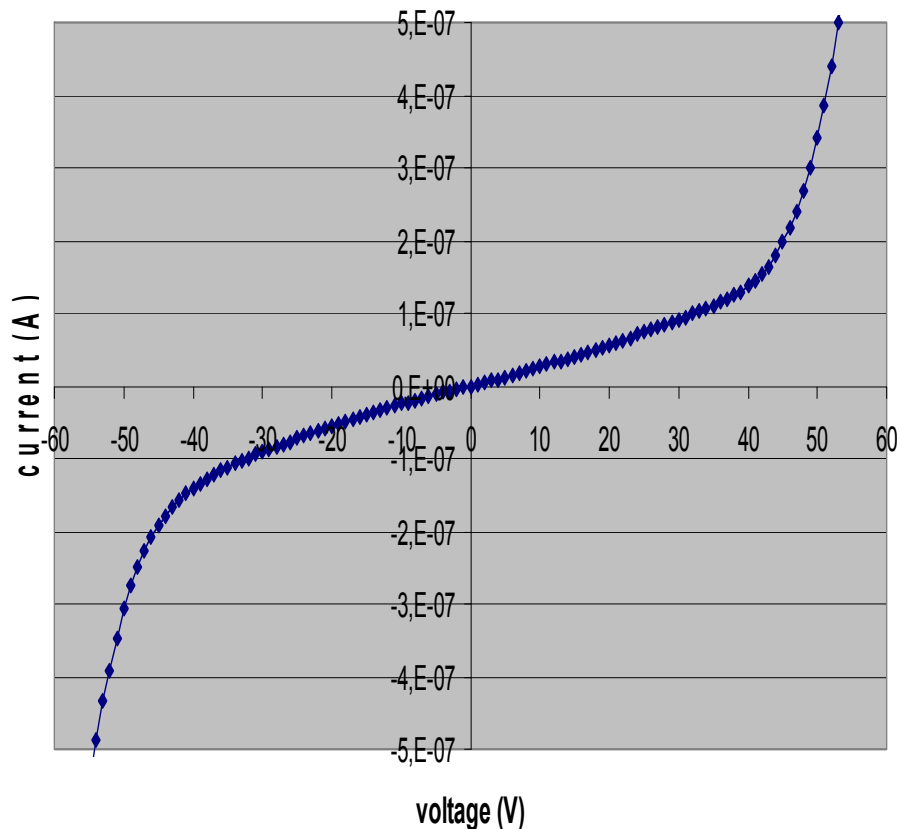
→ Evidenced in a $\log(I) = f(\log(V))$ diagram

- If $T_c < T_{\text{measurement}}$ $\gamma = 2$





sample 56173





i layer : Study of silane flow influence

| D= SiH ₄ /(SiH ₄ +H ₂) | SiH ₄ flux (sccm) | #num | Surface Xc (%) | Conductivity homogeneity | IV measurements observation |
|--|------------------------------|------|----------------|--------------------------|----------------------------------|
| 30% | 20 | 7821 | 28 | Not evaluated | High photogain, low dark current |
| 30% | 16 | 7823 | 27 | Not evaluated | Medium photogain & dark current |
| 30% | 12 | 7824 | 41 | Not evaluated | Low photogain, high dark current |
| 50% | 20 | 7825 | 36 | Bad | High photogain, low dark current |
| 50% | 16 | 7826 | 27 | Bad | Low photogain, high dark current |
| 50% | 12 | 7827 | 39 | Bad | Low photogain, high dark current |

- Samples 7821, 7825 (high silane flow)
 - High photogain (1000-10000), Low conductivity (10^{-11} - 10^{-9} S/cm)
 - ➔ amorphous Si dominates
- Decreasing the silane flow at the same dilution
 - Reduced photogain, increased dark conductivity
 - ➔ nc-Si dominates





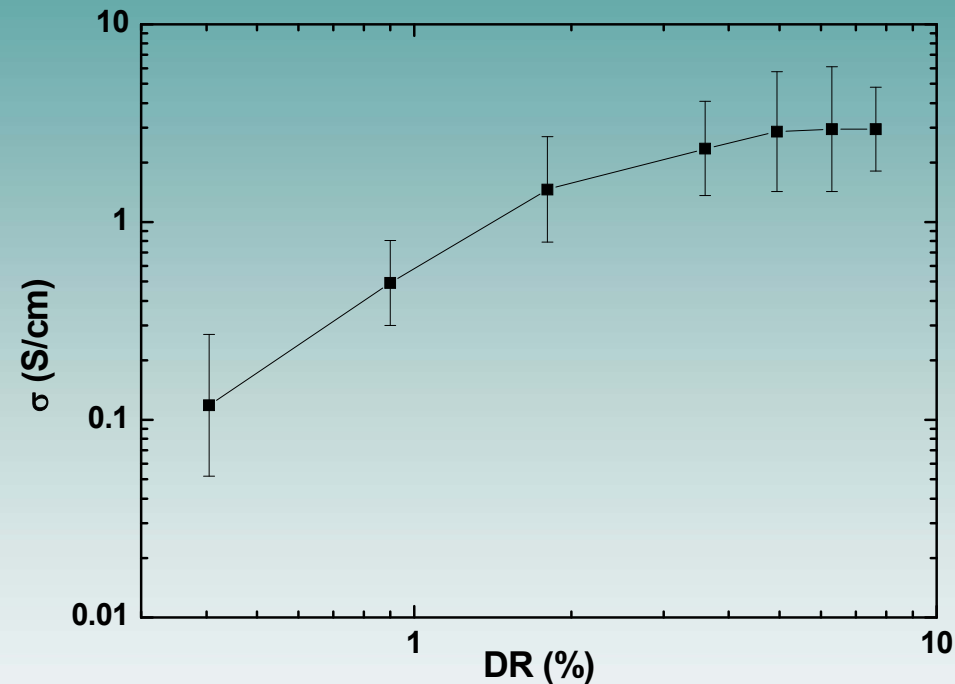
Ideal i layer conductivity characteristics for solar cells

- Bibliographic study establish that the best compromise between
 - Amorphous
 - Poor dark conductivity 10^{-11} - 10^{-9} S/cm (high recombination)
 - High photogain :1000-10000 : very good light absorption
 - And Crystalline silicon
 - High dark conductivity 10^{-4} - 10^{-5} S/cm (low recombination)
 - Low photogain :1-5 : low light absorption
 - Should be nc-Si with:
 - Medium dark conductivity 10^{-7} S/cm
 - Medium photogain : 100
- The best samples already grown show a dark conductivity of 10^{-8} S/cm for a photogain around 100
 - ➔ These samples will have lower electrical performance than the recommended ones from literature





Conductivity of p-type layers of series 8135-8144



- As expected the conductivity increases with doping ratio to reach a maximum of 5-6 S/cm at **DR 6.3%!!!**
In the literature the optimum DR is between 0.4 and 0.8% for VHF-PECVD or HWCVD
- The conductivity on one wafer varies for a factor 3 to 6
- With the averaging the maximum is not very pronounced





Microsharp environmental tests on samples coming from the wafer 7665 (Si substrate, $T=300^{\circ}\text{C}$, $d=30\%$)

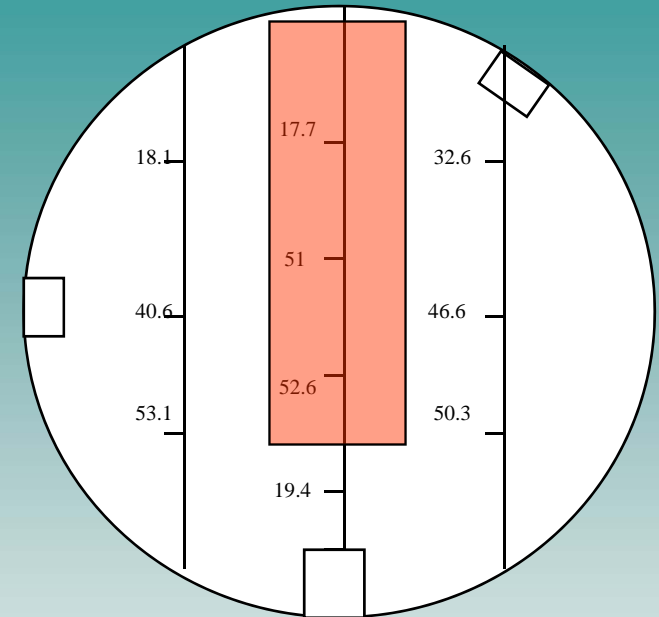
- 14 days @ 70°C and 95% Relative Humidity
- placed in dry oven @ 245°C for 14 days
- thermal shock from -35°C to 200°C for 3 days + thermal shock from -20°C and -30°C to 200°C for 3 days
- 14 days @ -40°C .





Results

- No crystallinity variation after tests
- hydrogen content decrease after TT in dry oven @ 245°C for 14 days



falls below the detection limit after

thermal shock from -35°C to 200°C for 3 days + thermal shock from -20°C and -30°C to 200°C for 3 days.





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Selection of **T**ransparent **C**onductive **O**xide

Requirement:

TCO must withstand plasma deposition of
Si layers

Results:

Indium tin oxide not stable against hydrogen
ZnO stable in plasma



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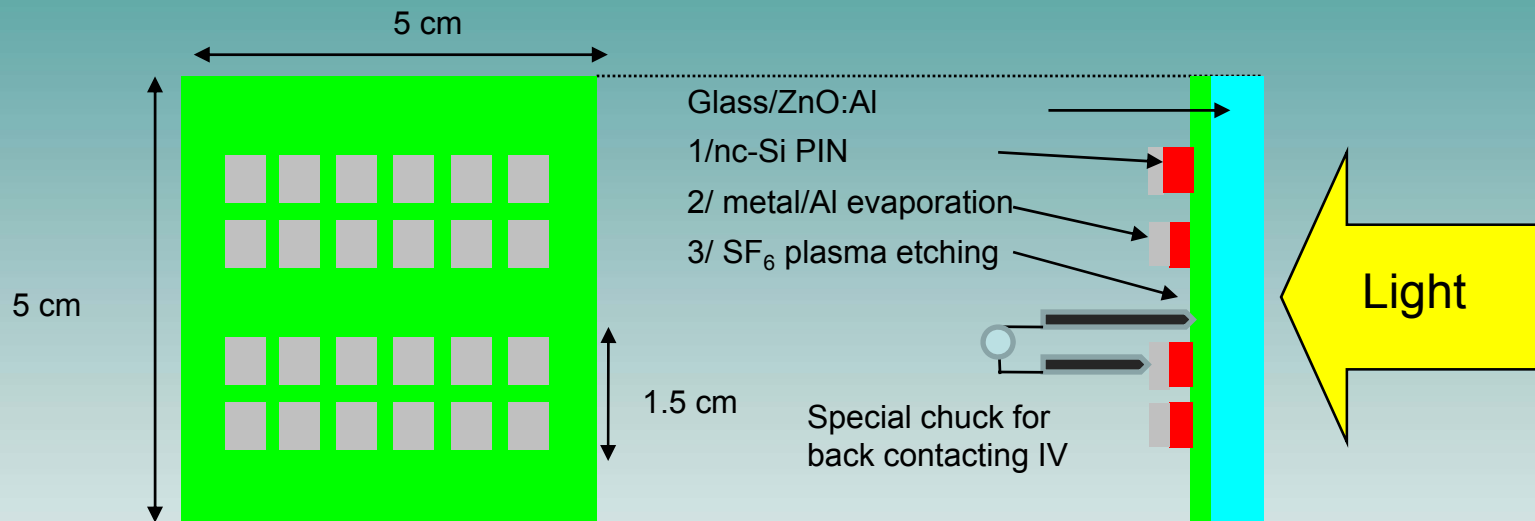


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20th November 2008/ L-NESS, Como



PIN solar cell global macroscopic structure elements and fabrication process

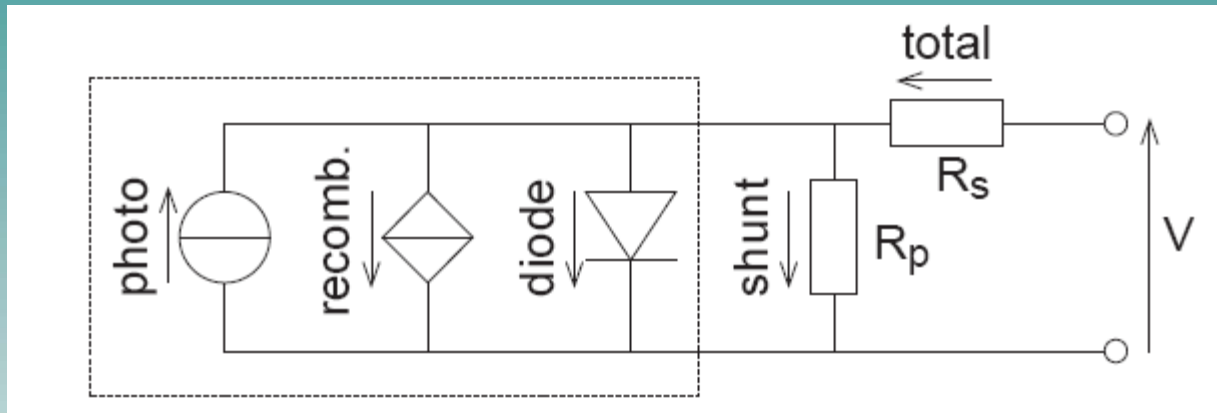


- Step 1/ pin nc-Si deposition at LNESS on glass/ZnO
- Step 2/ metal/Al evaporation (with mask)
- Step 3/ SF₆ plasma etching: removal of nc-Si between Al-contacts





IV curve model: Difference to wafer solar cells

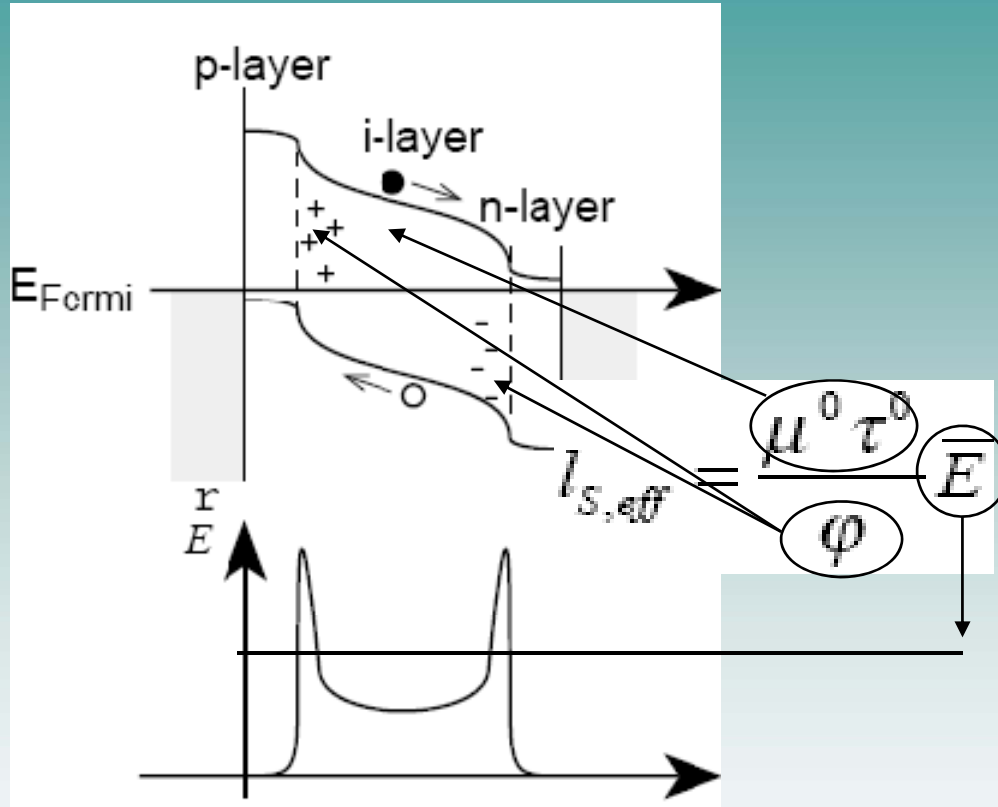


- Drift device: Carrier collection dependent on electric field between p-type and n-type layer
 - ideal diode factor = 2 (not 1)
 - diode saturation current $J_{on} \propto 1/\tau$ (not $1/\sqrt{\tau}$)
- Recombination current function of V
 - Merten collection model





Transport properties of the i-layer: Merten Model (1)



Assuming all that the diffusion is negligible Merten Hubin Crandall and Rech have express differently the **collection probability function** due to differing additional approximations

Hof remarked that these 4 models lead to similar results with different relative value of $\mu \cdot \tau$:

$$\mu^0 \tau^0|_{Crandall} + \mu^0 \tau^0|_{Rech} + \mu^0 \tau^0|_{Hubin} + \mu^0 \tau^0|_{Merten} \approx 1 + 2 + 3.73 + 4$$

(Phd Hof University of Neuchatel)

➔ Therefore these model are very suitable qualitatively while differing in the evaluation of $\mu \cdot \tau$ by a maximum factor of 4





Transport properties of the i layer: Merten Model (2)

$$I(V) = -I_{photo} \cdot \frac{1}{1 + \frac{L^2 \cdot \varphi}{\mu^0 \tau^0 \cdot (V_{bi} - [V - IR_s])}} + I_0 \left(e^{\frac{q(V - IR_s)}{nkT}} - 1 \right) + \frac{V - IR_s}{R_p}$$

generated current – recombination term
injection term (dark current)
shunt losses

$\mu_0 \cdot \tau_0$: Normalized mobility lifetime product: depend on electron and hole mobility and lifetime describes quality of the i layer

L: thickness of the i layer

φ : form factor: depend on the deformation of the electric field at the interface: quality of p/i and n/i interfaces (normaly between 1 and 2)

V_{bi} : build in voltage: depend on the activation energy of n and p layer :doping efficiency of n and p layer (assumed to be around 1V)

 **current increasing linearly in reverse bias, independently from the parallel resistance due to increased collection of generated carriers**






Transport properties of the i-layer: Dependence of I_{photo} on L

$$I(V) = -I_{photo} \cdot \frac{1}{1 + \frac{L^2 \cdot \phi}{\mu^0 \tau^0 \cdot (V - IR_s)}} + I_0 \left(e^{\frac{q(V - IR_s)}{nkT}} - 1 \right) + \frac{V - IR_s}{R_p}$$

generated current - recombination term
injection term (dark current)
shunt losses



The recombination increase with L however the generation increase also with L

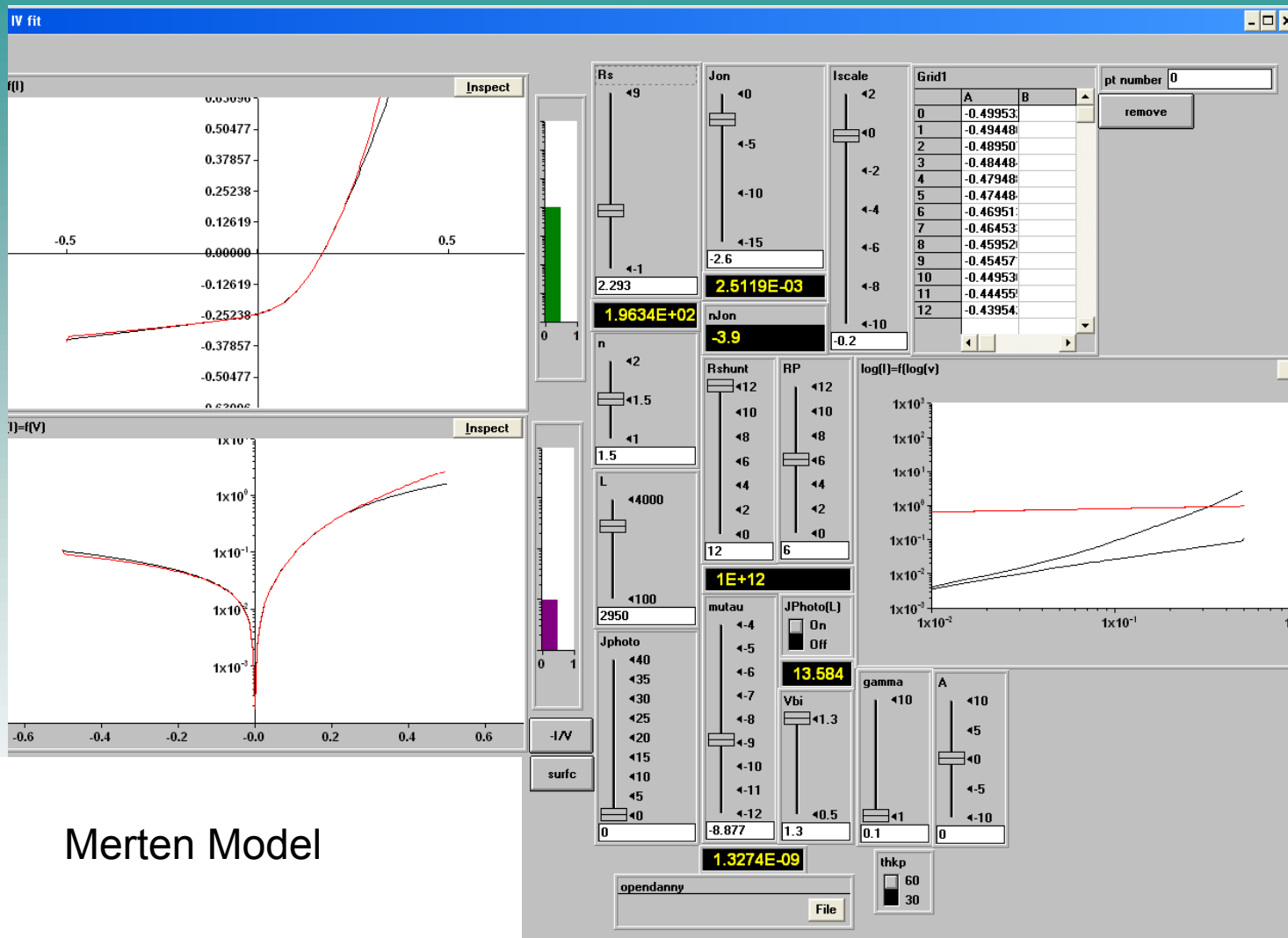
→ Simulation of the absorption of the i layer varying L with **Optical** considering:

- Low roughness for all layers : 5nm
- X_c 50%

→ Convolution with solar spectrum lead to I_{photo} :

Fitted with very good accuracy by an empirical law: $I_{photo} = A + B \cdot \log(L + C)$







First series of pin nc-Si devices

Device design

Ag/Al contact, *pin* Si layer thickness: 30 nm / 1 μ m / 80 nm

Technological results:

Contact metal defoliates, hardly any contact to Si

Electrical results

Supralinear behaviour in reverse bias

- Can be modelized by power law > 2

→ SCLC(T_c correct, correct layer)

→ i-layer is contacted directly, non existing p layer

Next series

- Thicker p-type and n-type layers as well as different i-layer thicknesses

- Ti / Pd / Ag / Al contact





Second series of pin nc-Si devices

Device design

Ti / Pd / Ag / Al contact, *pin* Si layer thickness: 60 nm / 1 or 2 μm / 150 nm

Technological results:

Contacts OK, thickness check by transmission: 1.475 and 2.950 μm

Electrical results

1 μm i-layer: all cells shunted, no SCLC

2 μm i-layer: 4/10 not shunted

$\mu^0\tau^0/\phi$: improved, p-type and n-type doping OK as deduced from V_{BI} fits

J_{on} significantly lower than in series 1

Next series

- ➔ Keep device design
- ➔ Slower growth for higher Si layer quality, introduce p/i and n/i buffer





Third series of pin nc-Si devices „16 sccm“

Device design

Ti / Pd / Ag / Al contact, *pin* Si layer thickness: 60 nm / 1 or 2 μm / 150 nm

Technological results:

Contact resistance high

Electrical results

Higher V_{OC} corresponding to lower crystalline fraction

$\mu^0\tau^0/\phi$: improved further, material has higher quality

J_{on} significantly lower than in series 2

Shunt problems: may be due to pin holes





Third series of pin nc-Si devices „3 sccm“

Device design

Ti / Pd / Ag / Al contact, *pin* Si layer thickness: 60 nm / 1 or 2 μm / 150 nm

Technological results:

Contact resistance high

Electrical results

Lower V_{OC} corresponding to higher crystalline fraction

$\mu^0\tau^0/\phi$: improved further, material has higher quality

J_{on} significantly lower than in series 2

Shunt problems: may be due to pin holes





Conclusion

- Electrical properties of i-layer and p-type layer determined
- Environmental testing on LE-PECVD Si layers carried out
- First LE-PECVD based PIN Solar cells are fabricated
- New input for further layer and interface optimization gained by in depth characterisation

